**1. (Currently Amended)** A packaging process for a semiconductor package, comprising the steps of:

1) preparing a substrate having a first surface and a second surface, wherein at least one chip-mounting area is formed on the first surface with the first surface having a first plurality of bond pads formed in the substrate and are electrically connected to the substrate;

2) screen printing a plurality of conductive elements on the chip-mounting area of the substrate in direct alignment over each of said first plurality of bond pads, wherein the conductive elements are electrically connected to the substrate and each formed with a flat end;

3) forming a first encapsulant by a printing process on the chip-mounting area of the substrate for encapsulating the conductive elements, wherein the first encapsulant formed by printing is adapted to have a top surface thereof formed in coplanar alignment with the flat ends of the conductive elements to thereby form a common coplanar surface, and the ends of the conductive elements are exposed to the outside of the first encapsulant;

4) preparing at least one semiconductor chip having a second plurality of bond pads formed on a surface thereof, and mounting the semiconductor chip on the top surface of the first encapsulant in a manner that the second bond pads are electrically connected to the exposed ends of the conductive elements respectively and with the surface of the semiconductor chip closely attached to the coplanar surface formed by the first encapsulant and conductive elements free of any gap between the semiconductor chip and the coplanar surface;

5) forming a second encapsulant on the first surface of the substrate for encapsulating the chip; and

6) implanting a plurality of solder balls on the second surface of the substrate, wherein the solder balls are electrically connected to the substrate.

**2. (Original)** The packaging process of claim 1, wherein the conductive elements are conductive bumps.

**3. (Original)** The packaging process of claim 2, wherein the conductive bumps are made of tin, lead or tin/lead alloy.

**4. (Cancelled)**

**5. (Cancelled)**

**6. (Original)** The packaging process of claim 1, wherein the chip has a surface with no bond pads formed thereon encapsulated by the second encapsulant.

**7. (Original)** The packaging process of claim 1, wherein the chip has a surface with no bond pads formed thereon exposed to the outside of the second encapsulant for directly contacting the atmosphere.

**8. (Previously Amended)** The packaging process of claim 1, further comprising a step of attaching a heat sink to the first surface of the substrate after the step (4) of mounting the chip on the first encapsulant, allowing the heat sink to be encapsulated by the second encapsulant in the step (5) of forming the second encapsulant.